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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/766,210	01/29/2004	Yong-Kwan Lee	2557-000202/US	3354

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EXAMINER	
HO, TU TU V	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 02/18/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

A2

Office Action Summary	Application No.	Applicant(s)	
	10/766,210	LEE ET AL.	
	Examiner	Art Unit	
	Tu-Tu Ho	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 January 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) *6 and 7* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5 and 8-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 January 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *01/29/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Oath/Declaration

1. The oath/declaration filed on 08/12/2004 is acceptable.

Election/ Restriction

2. Applicant's election without traverse of Species IA, **claims 1-5 and 8-16**, within elected Invention I, and cancellation of Invention II, claims 17-30, in the reply filed on 01/24/2005 is acknowledged.

3. **Claims 6-7** are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected species, there being no allowable generic or linking claim. Election was made **without** traverse as noted above.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in
> (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or
> (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. **Claims 1-2, 4, 8, and 16** are rejected under 35 U.S.C. 102(b) as being anticipated by Sherif et al. U.S. Patent 5,623,394 (the '394 patent).

The '394 patent discloses in Figs. 1-2 and respective portion of the specification a flip chip package as claimed.

Referring to **claim 1**, the reference discloses a flip chip package comprising:

a semiconductor chip (41) having a first side and a second side opposing the first side;

a circuit substrate (10) electrically connected to the first side of the semiconductor chip;

a protective cap (25 or 35) disposed over the second side of the semiconductor chip, the protective cap including at least one portion extending beyond an edge of the semiconductor chip (as is evident from the figures).

Referring to **claim 2**, the reference further discloses that the protective cap includes metal (column 6, lines 25-26).

Referring to **claim 4**, the reference further discloses a plurality of solder bumps (22) to electrically connect the semiconductor chip and the circuit substrate.

Referring to **claim 8**, the reference further discloses an adhesion layer ("thermal paste" 51) disposed between the second side of the semiconductor chip and the protective cap (column 7, lines 30-35).

Referring to **claim 16**, the reference further discloses solder balls (12) formed on a surface of the circuit substrate opposite a surface to which the circuit substrate is electrically connected to the semiconductor chip.

5. **Claims 1-5, 8-11, 13-14, and 16** are rejected under 35 U.S.C. 102(b) as being anticipated by Johnson U.S. Patent 5,726,079 (the '079 patent).

The '079 patent discloses in Fig. 1 and respective portion of the specification a flip chip package as claimed.

Referring to **claim 1**, the reference discloses a flip chip package comprising:

a semiconductor chip (12) having a first side and a second side opposing the first side;

a circuit substrate (16) electrically connected to the first side of the semiconductor chip;

a protective cap ("thermally conductive planar member" 22, column 2, lines 49-51, and note that although the reference does not explicitly disclose that element 22 is a protective cap, it is a protective cap as it protects the chip from the environmental elements) disposed over the second side of the semiconductor chip, the protective cap including at least one portion extending beyond an edge of the semiconductor chip (as is evident from the figure).

Referring to **claim 2**, the reference further discloses that the protective cap includes metal (column 3, lines 24-26).

Referring to **claim 3**, the reference's material (copper, column 3, lines 24-26) for the protective cap meets the materials of the Markush group of the claim.

Referring to **claim 4**, the reference further discloses a plurality of solder bumps (14) to electrically connect the semiconductor chip and the circuit substrate.

Referring to **claims 5 and 9**, the reference further discloses a molding resin layer (26) sealing the electrical connection between the semiconductor chip and the circuit substrate.

Referring to **claim 8**, the reference further discloses an adhesion layer (28, column 3, lines 20-23) disposed between the second side of the semiconductor chip and the protective cap.

Referring to **claim 10**, the reference further discloses that the molding resin layer engages the extended portion of the protective cap ("the extended portion of the protective cap" is interpreted as the "portion extending beyond an edge of the semiconductor chip" of claim 1).

Referring to **claims 11, 13, and 14**, the reference implicitly discloses, as evident from the figure, that the molding resin layer at least assists in mounting the protective cap over the second side of the semiconductor chip and that said assisting is by engaging the molding resin layer with the protective cap.

Referring to **claim 16**, the reference further discloses solder balls (12) formed on a surface of the circuit substrate opposite a surface to which the circuit substrate is electrically connected to the semiconductor chip.

6. **Claims 1, 4, 5, 8, 9, and 16** are rejected under 35 U.S.C. 102(e) as being anticipated by Tsao et al. U.S. Patent 6,607,942 (the '942 patent).

The '942 patent discloses in Fig. 4b and respective portion of the specification a flip chip package as claimed.

Referring to **claim 1**, the reference discloses a flip chip package comprising:

a semiconductor chip (12) having a first side and a second side opposing the first side;

a circuit substrate (10) electrically connected to the first side of the semiconductor chip;

a protective cap ("heat spreader" 44, column 4, lines 49-55, and note that although the reference does not explicitly disclose that element 44 is a protective cap, it is a protective cap as it protects the chip from the environmental elements) disposed over the second side of the

semiconductor chip, the protective cap including at least one portion extending beyond an edge of the semiconductor chip (as is evident from the figure).

Referring to **claim 4**, the reference further discloses a plurality of solder bumps (11) to electrically connect the semiconductor chip and the circuit substrate.

Referring to **claims 5 and 9**, the reference further discloses a molding resin layer (13, column 4, lines 5-15) sealing the electrical connection between the semiconductor chip and the circuit substrate.

Referring to **claim 8**, the reference further discloses an adhesion layer (15, column 4, lines 5-15) disposed between the second side of the semiconductor chip and the protective cap.

Referring to **claim 16**, the reference further discloses solder balls (26) formed on a surface of the circuit substrate opposite a surface to which the circuit substrate is electrically connected to the semiconductor chip.

7. **Claims 1-5, 8-11, 13-14, and 16** are rejected under 35 U.S.C. 102(e) as being anticipated by Caletka et al. U.S. Patent 6,507,116 (the '116 patent).

The '116 patent discloses in the figures, particularly Fig. 4, and respective portion of the specification a flip chip package as claimed.

Referring to **claim 1**, the reference discloses a flip chip package comprising:

a semiconductor chip (12, Fig. 1, no number in Fig. 4) having a first side and a second side opposing the first side;

a circuit substrate (16, Fig. 1 or 216, Fig. 4) electrically connected to the first side of the semiconductor chip;

a protective cap ("thermally conductive member" 222, Fig. 4, column 6, lines 31-47, and note that although the reference does not explicitly disclose that element 222 is a protective cap, it is a protective cap as it protects the chip from the environmental elements) disposed over the second side of the semiconductor chip, the protective cap including at least one portion extending beyond an edge of the semiconductor chip (as is evident from the figures).

Referring to **claim 2**, the reference further discloses that the protective cap includes metal (column 5, lines 5-10).

Referring to **claim 3**, the reference further discloses that the protective cap is made of one selected from the group consisting of copper (Cu), copper alloy, aluminum (Al), and aluminum alloy (column 5, lines 5-10).

Referring to **claim 4**, the reference further discloses a plurality of solder bumps (214) to electrically connect the semiconductor chip and the circuit substrate.

Referring to **claims 5 and 9**, the reference further discloses a molding resin layer (226) sealing the electrical connection between the semiconductor chip and the circuit substrate.

Referring to **claim 8**, the reference further discloses an adhesion layer (also as 226 in Fig. 4, and in Fig. 1, as 26, column 5, lines 30-35) disposed between the second side of the semiconductor chip and the protective cap.

Referring to **claim 10**, the reference further discloses that the molding resin layer engages the extended portion of the protective cap ("the extended portion of the protective cap" is interpreted as the "portion extending beyond an edge of the semiconductor chip" of claim 1).

Referring to **claims 11, 13, and 14**, the reference discloses that the molding resin layer at least assists (column 6, lines 40-45) in mounting the protective cap over the second side of the

semiconductor chip and that said assisting is by engaging the molding resin layer with the protective cap.

Referring to **claim 16**, the reference further discloses solder balls (Fig. 1, no number) formed on a surface of the circuit substrate opposite a surface to which the circuit substrate is electrically connected to the semiconductor chip.

Claim Rejections - 35 USC § 102 or 103

The following is a quotation of 35 U.S.C. §103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. **Claims 12 and 16** are rejected under 35 U.S.C. 102(e) as being anticipated by or, in the alternative, under 35 U.S.C. §103(a) as being obvious over the '116 patent.

The '116 patent discloses a flip chip package as claimed and as detailed above including the protective cap 222 having a groove 229 in the extended portion and further discloses that the molding resin layer 226 includes a groove portion (also 226) disposed in the groove. The reference further discloses that the groove could be a circular shape or could be many other shapes such as, for example, diamond or hexagonal shapes (column 6 lines 40-50). However, the reference fails to disclose that the groove is a dovetail groove as claimed. Nevertheless, the limitation (dovetail), if interpreted broadly ("a joint formed by interlocking tenons and mortises", Compact Oxford English Online Dictionary), is anticipated by the disclosed interlocking tenon

226 and mortise 229; in the alternative, the disclosed diamond or hexagonal shapes for the groove is functionally equivalent to the claimed dovetail groove, therefore the change from one shape to the other would have been obvious to one of ordinary skill in the art at the time the invention was made.

Conclusion

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tu-Tu Ho whose telephone number is (571) 272-1778. The examiner can normally be reached on 6:30 am - 5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, DAVID NELMS can be reached on (571) 272-1787. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Tu-Tu Ho
February 11, 2005